Microcontroller (EEC421)

Lecture 3

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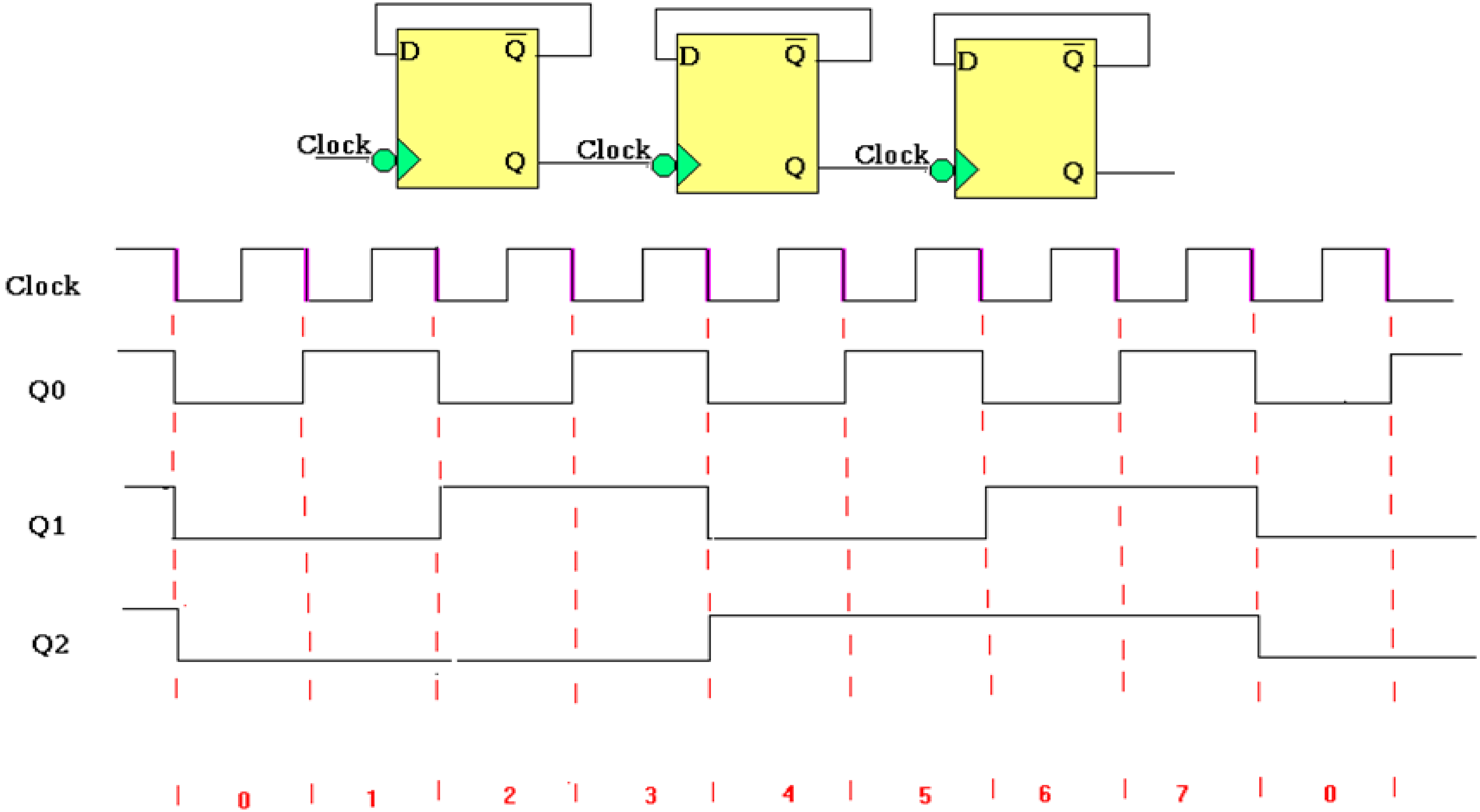
1- DC Machines

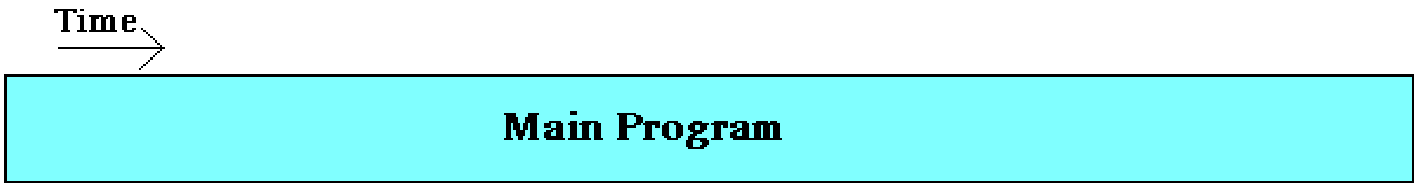
- ❑ **<u>Lecture 2: THE 8051 ARCHITECTURE</u>**
- ✓ 8051 Microcontroller Hardware
- ✓ Counters, Registers, Memory
- ✓ Input / Output Pins, Ports, and Circuits
- ✓ Timers, Serial data

Timer:



Interrupt :

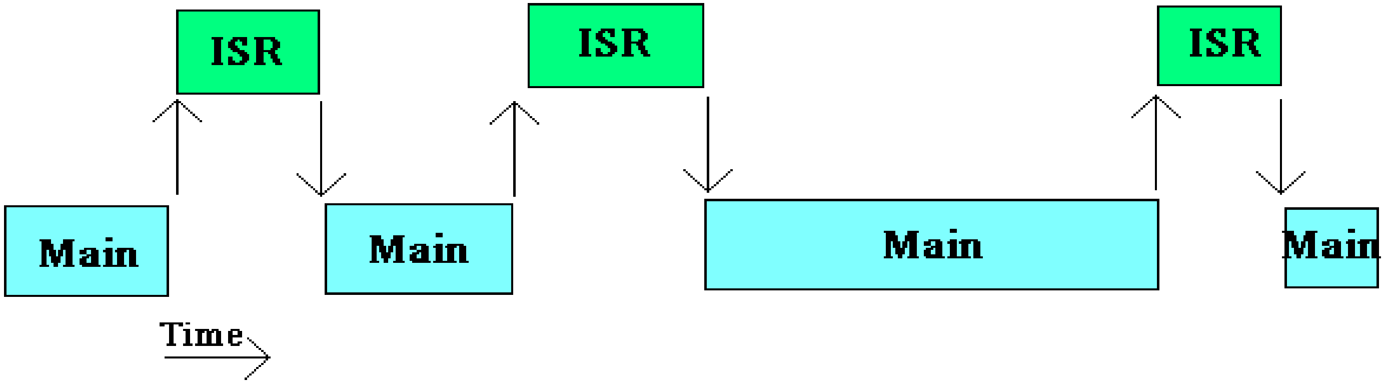
Program execution without intrrupts :



Time

Main Program

Program execution with intrrupts :



ISR

ISR

ISR

Main

Main

Main

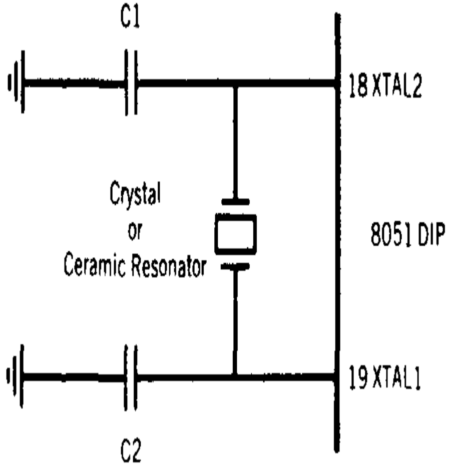
Main

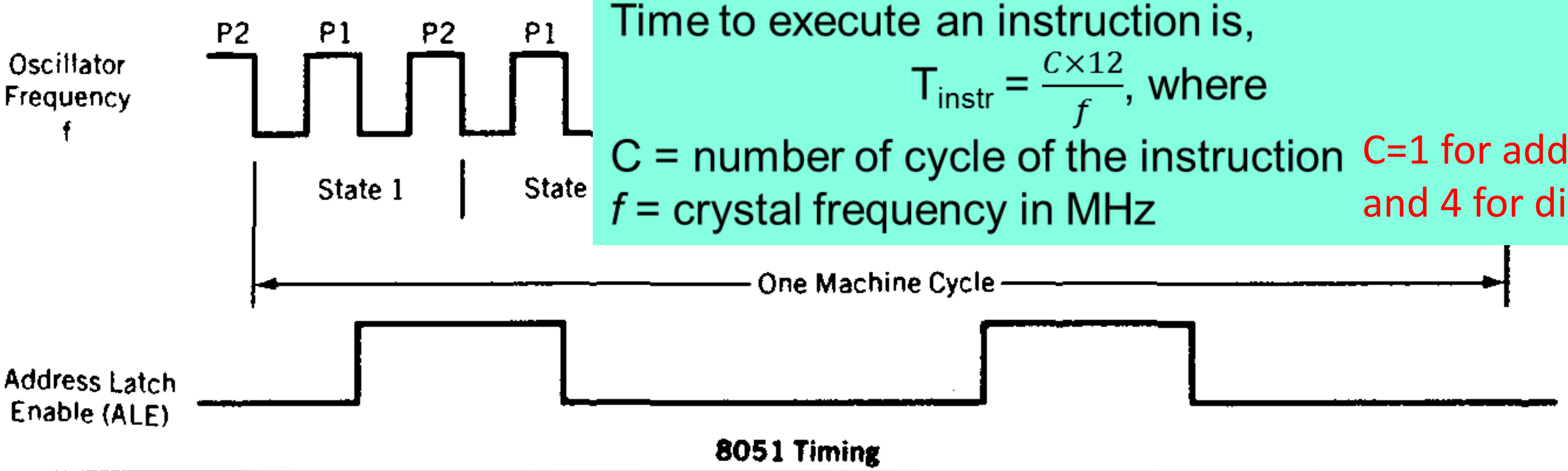
Time

ISR : Intrrupt Service Routin

Clock/Oscillator

- Clock and communication requirement
- Ceramic or crystal?
- State=2 pulses
- Machine cycle=6 states
- Instruction cycle=1/2/4 MC depends on type of instruction.





8051 Timing

Time to execute an instruction is,

$$T_{instr} = \frac{C\times 12}{f}, \text{ where}$$

C = number of cycle of the instruction

f = crystal frequency in MHz

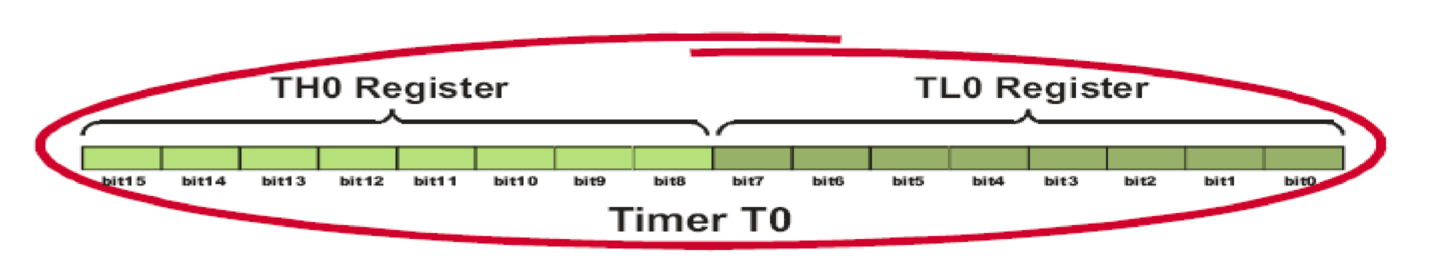
C=1 for add inst. and 4 for div. inst.

Timers/counters

- Event detection, timed control signal generation, counter etc.
- Reads from or written to by the processor and is given by some constant frequency source. Generates an interrupt at the overflow. Run by µC clock or external clock.

Timer/counter contd..

- A machine cycle instruction lasts for 12 quartz oscillator periods, which means that by embedding quartz with oscillator frequency of 12MHz, a number stored in the timer register will be changed million times per second, i.e. each microsecond.
- 2 timers/counters called T0 and T1



- If the timer contains for example number 1000 (decimal), then the TH0 register (high byte) will contain the number 3, while the TL0 register (low byte) will contain decimal number 232.
- Formula: TH0 × 256 + TL0 = T

so, 3 × 256 + 232 = 1000

TH0 = 1000/256 = 3 (00000011)

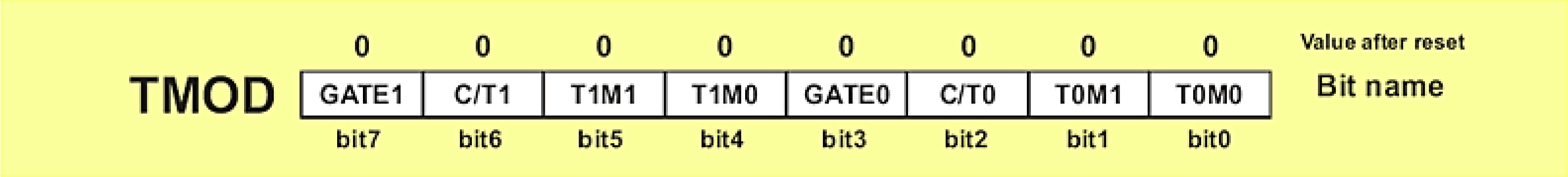
TL0 = 1000 – 3x256 = 232 (11101000)

Timer/counter contd..

- The largest value it can store is 65 535
- In case of exceeding this value, the timer will be automatically cleared and counting starts from 0. This condition is called an overflow.

TMOD Register (Timer Mode)

- There are 4 operational modes.



	0	0	0	0	0	0	0	0	Value after reset
TMOD	GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0	Bit name
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	

- The low 4 bits (bit0 - bit3) refer to the timer 0, while the high 4 bits (bit4 - bit7) refer to the timer 1.
- **GATE1** enables and disables Timer 1 by means of a signal brought to the INT1 pin (P3.3):
  - **1** - Timer 1 operates only if the INT1 bit is set.
  - **0** - Timer 1 operates regardless of the logic state of the INT1 bit.
- **C/T1** selects pulses to be counted up by the timer/counter 1:
  - **1** - Timer counts pulses brought to the T1 pin (P3.5).
  - **0** - Timer counts pulses from internal oscillator.
- **T1M1,T1M0** These two bits select the operational mode of the Timer 1.

T1M1	T1M0	MODE	DESCRIPTION
0	0	0	13-bit timer
0	1	1	16-bit timer
1	0	2	8-bit auto-reload
1	1	3	Split mode

GATE0 enables and disables Timer 1 using a signal brought to the INT0 pin (P3.2):

1 - Timer 0 operates only if the INT0 bit is set.

0 - Timer 0 operates regardless of the logic state of the INT0 bit.

C/T0 selects pulses to be counted up by the timer/counter 0:

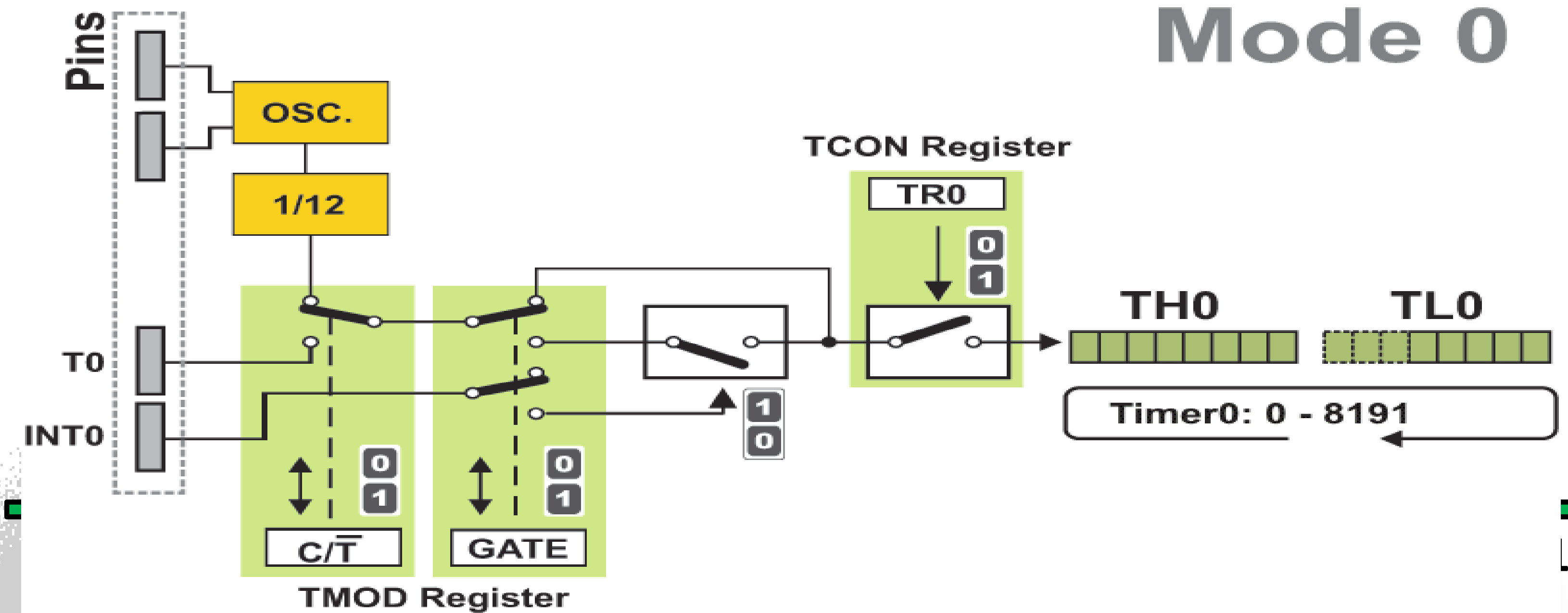
1 - Timer counts pulses brought to the T0 pin (P3.4).

0 - Timer counts pulses from internal oscillator.

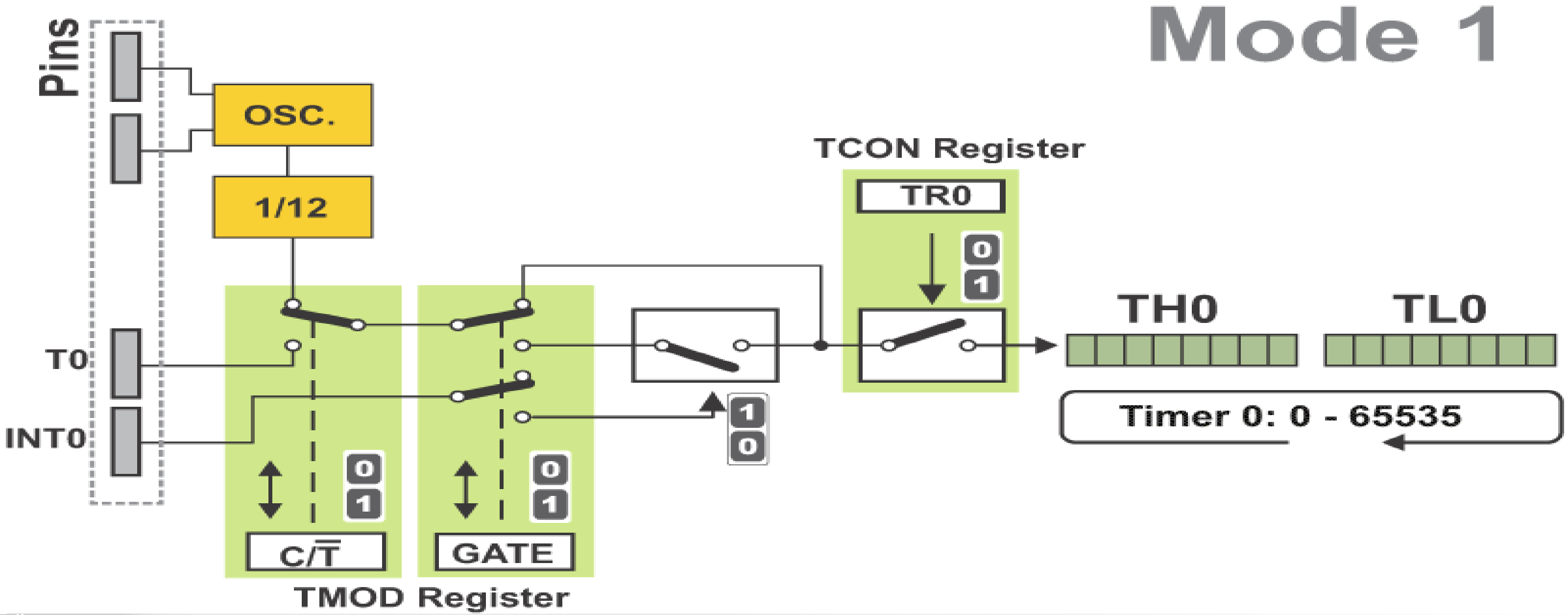
T0M1,T0M0 These two bits select the operational mode of the Timer 0.

T0M1	T0M0	MODE	DESCRIPTION
0	0	0	13-bit timer
0	1	1	16-bit timer
1	0	2	8-bit auto-reload
1	1	3	Split mode

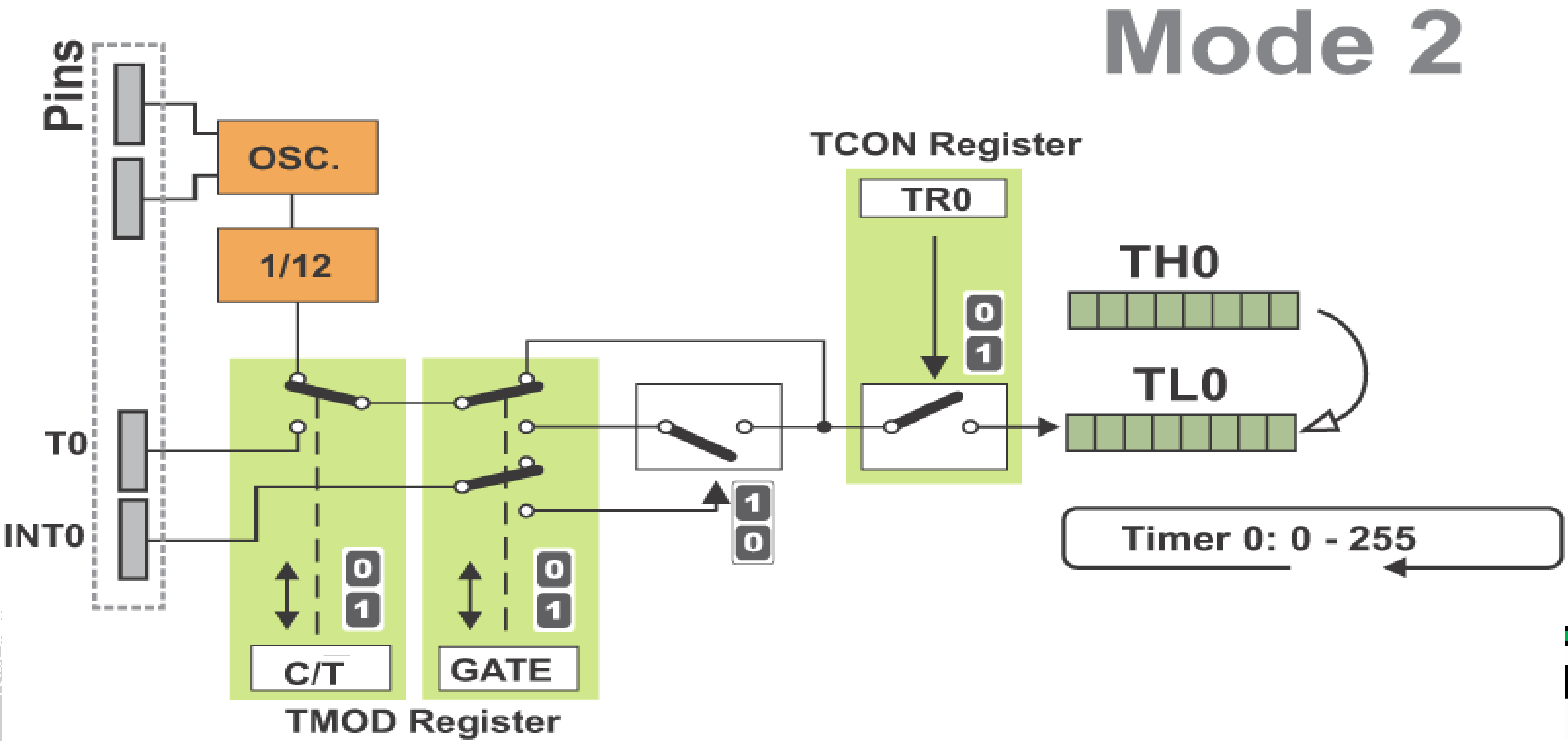
- Timer 0 in mode 0 (13-bit timer):
  - This mode configures timer 0 as a 13-bit timer which consists of all 8 bits of TH0 and the lower 5 bits of TL0. As a result, the Timer 0 uses only 13 of 16 bits. Each coming pulse causes the lower register bits to change their states. After receiving 32 pulses, this register is loaded and automatically cleared, while the higher byte (TH0) is incremented by 1. This process is repeated until registers count up 8192 pulses. After that, both registers are cleared and counting starts from 0.



- Timer 0 in mode 1 (16-bit timer)
  - Mode 1 configures timer 0 as a 16-bit timer comprising all the bits of both registers TH0 and TL0. That's why this is one of the most commonly used modes. Timer operates in the same way as in mode 0, with difference that the registers count up to 65 536 as allowable by the 16 bits.

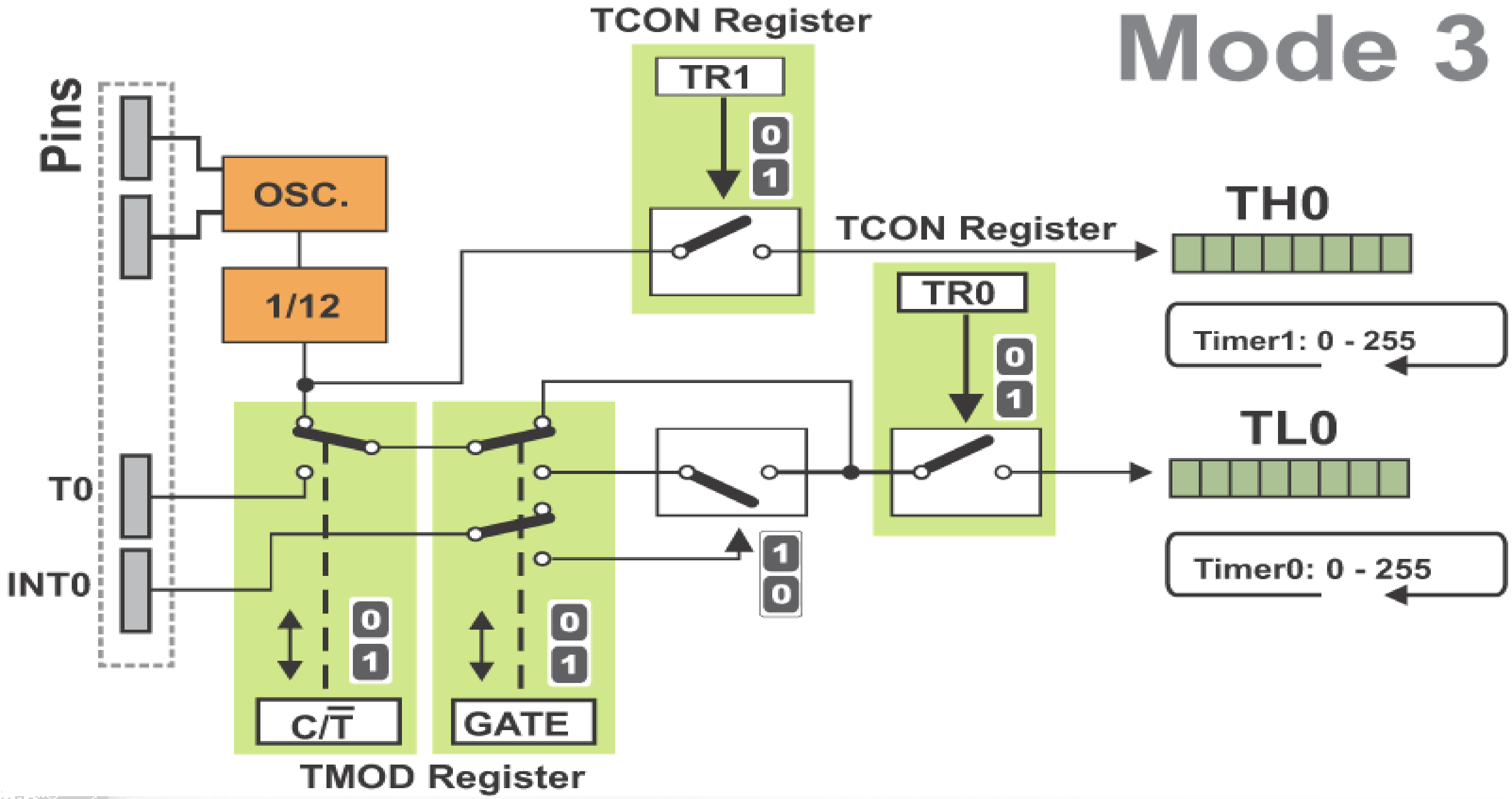


- Timer 0 in mode 2 (Auto-Reload Timer)
  - Mode 2 configures timer 0 as an 8-bit timer. Actually, timer 0 uses only one 8-bit register for counting and never counts from 0, but from an arbitrary value (0-255) stored in another (TH0) register.

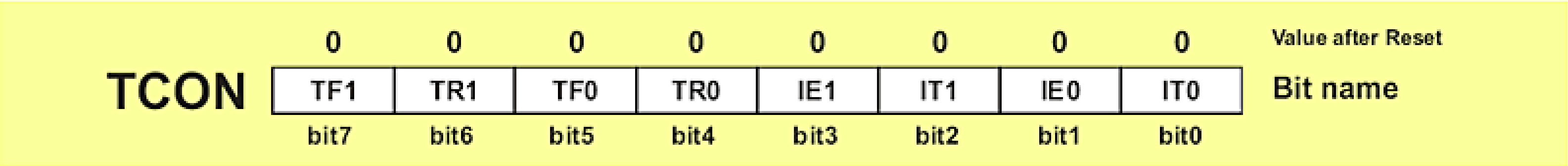


- **Timer 0 in Mode 3 (Split Timer)**
  - Mode 3 configures timer 0 so that registers TL0 and TH0 operate as separate 8-bit timers. In other words, the 16-bit timer consisting of two registers TH0 and TL0 is split into two independent 8-bit timers.
  - This mode is provided for applications requiring an additional 8-bit timer or counter. The TL0 timer turns into timer 0, while the TH0 timer turns into timer 1. In addition, all the control bits of 16-bit Timer 1 (consisting of the TH1 and TL1 register), now control the 8-bit Timer 1. Thus, the operation 16 bit timer 1 is restricted when timer 0 is in mode 3.

- **Timer 0 in Mode 3 (Split Timer)**



Timer Control (TCON) Register

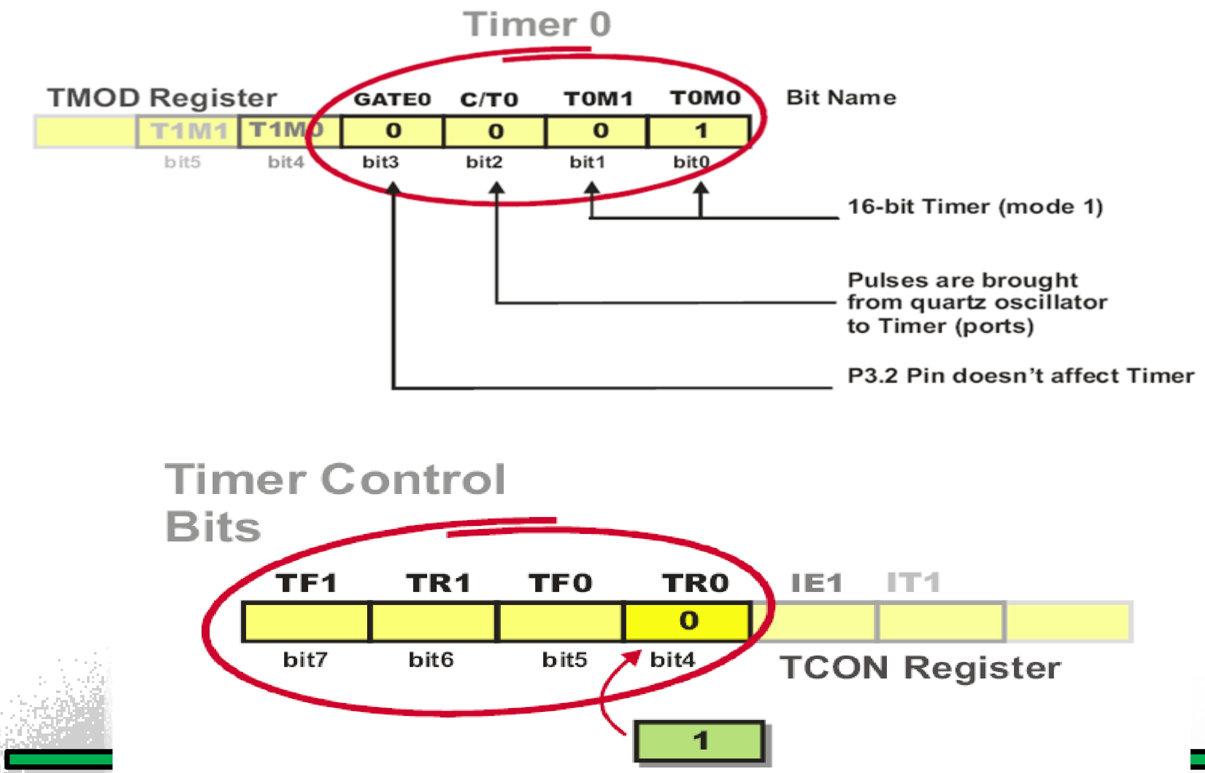
- Only 4 bits of this register are used for this purpose, while rest of them is used for interrupt control.
- 

TCON									
	0	0	0	0	0	0	0	0	Value after Reset
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	Bit name
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	

- **TF1** bit is automatically set on the Timer 1 overflow.
- **TR1** bit enables the Timer 1.
  - **1** - Timer 1 is enabled.
  - **0** - Timer 1 is disabled.
- **TF0** bit is automatically set on the Timer 0 overflow.
- **TR0** bit enables the timer 0.
  - **1** - Timer 0 is enabled.
  - **0** - Timer 0 is disabled.

How to use the Timer 0 ?

- the timer 0 operates in mode 1 and counts pulses generated by internal clock the frequency of which is equal to 1/12 the quartz frequency.



Timer 0 Overflow Detection

- When it occurs, the TF0 bit of the TCON register will be automatically set.
- The state of this bit can be constantly checked from within the program or by enabling an interrupt which will stop the main program execution when this bit is set.
- a program delay of 0.05 seconds (50 000 machine cycles).